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James Richard Shealy

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Cornell University
373 Pine Tree Rd, EHP
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14. ABSTRACT

This program was focused on the development of alternative and superior dielectric passivations to AlGaN/GaN HEMT transistors for mm- wave operation. A new process was developed to deposit by LPCVD the composite dielectric of AlSiN containing as much as 10 atomic % by weight of aluminum. This dielectric partially depletes the 2DEG which has be effectively used in place of a gate extension. The resulting devices do not display non-linear increases in access resistances, and they deliver state-of-the-art power performance at large drain bias at frequencies up to 10 and 35 GHz.

15. SUBJECT TERMS

GaN, MODFETs, Microwave power FETs, passivation

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Performance of AlGaN/GaN High Electron Mobility Transistors with AlSiN Passivation

Ekaterina Harvard, Richard Brown, and James R. Shealy

Abstract

The performance of AlGaN/GaN High Electron Mobility Transistors passivated with AlSiN and SiN, and fabricated side-by-side has been studied. It is found that the AlSiN passivation produced state of the art devices, improving both small and large signal performance over the SiN passivation, particularly at higher drain bias. With large signal excitation at 10 GHz, the effects of second harmonic termination on the load-pull were also studied. Significant improvements in the power-added efficiency were demonstrated.

Index Terms

GaN, MODFETs, Microwave power FETs, passivation.

I. Introduction

THE AlGaN/GaN HEMT has been studied for its high power handling capability and applications in microwave sources and power amplifiers, as well as MMICS [1]–[4]. State of the art devices have delivered over 30 W/mm of output power at 8 GHz [5], 16 W/mm at 10 GHz [6], and 10 W/mm at 40 GHz [7]. Devices with short gate lengths (30 nm) have shown cutoff frequencies (f_T) of 180 GHz [8]. Furthermore, high-efficiency amplifiers have been produced with power-added efficiency (PAE) exceeding 75 % [9].

Surface passivation has been shown to play a key role in reducing surface trapping and dispersion in the channel [10]. However, this layer increases the gate-source capacitance (a key parasitic), and creates a resistive shunt in both the gate-source and gate-drain circuits. Thus, a dielectric that adequately passivates the surface without creating large parastitic resistances and capacitances would be ideal. This work presents a comparison between two passivation materials, SiN and AlSiN, on side-by-side fabricated devices. Each dielectric was deposited by a high temperature LPCVD process to a thickness of roughly 30 nm producing low defect, hydrogen-free (relative to more common methods) films. AlSiN was used due to its larger bandgap and its expected lower permittivity at microwave frequencies. Comparisons of both small- and large-signal performance were carried out. For small-signal measurements, the device model described by Shealy *et. al.* [11] was used for extracting the device parameters. These parameters and model were also used to predict the effects of various parasitic elements on the small-signal performance of the device, especially the cut-off frequencies f_T and f_{max}.

A significant second harmonic component at the output when the device was biased near pinch off allowed for study of the effects of harmonic loading. The theory of harmonic loading [12] has been studied in computer simulation [13] and

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The authors are with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853. (email: eh348@cornell.edu)

demonstrated in many experiments. The effects of the higher order harmonics produced by the device have been documented both at the input [14] and output [15]–[20].

Theoretical analysis states that the power-added efficiency can be improved by 5-10 % by terminating the second harmonic in a short, which reflects the in-phase second harmonic power back to the device in the opposite phase, allowing it to contribute to the fundamental power [12]. Experiments on recent devices reflect this range, where improvements of PAE of 4.1 % [15] to as much as 10 % [19] have been reported.

II. Fabrication

AlSiN and SiN films were deposited in a modified low-pressure chemical vapor deposition (LPCVD) system onto etched mesa-isolated AlGaN/GaN HEMT structures with 25 nm $Al_{0.25}Ga_{0.75}N$ barriers grown on S.I. SiC. Dielectric deposition was performed at 750 °C at a pressure of 2 Torr with Trimethylaluminum, Dichlorosilane, and Ammonia as precursors. The conditions for deposition of the SiN films were adjusted to produce low stress, slightly Si rich films. The Aluminum fraction (controlled by the Trimethylaluminum flux) of the AlSiN dielectrics was measured to be ~6 at. % by X-Ray Photoelectron Spectroscopy. SiN passivated structures had a full channel charge $\sim 1.6 \times 10^{13}$ cm^{-2} with a corresponding sheet resistance of ~450 Ω/square. Ta/Ti/Al/Mo/Au source/drain, and Ni/Au gate contacts were placed in etched windows through the dielectric using CF_4, and $SF_6/BCl_3/Ar$ RIE etches, respectively, defined by electron beam lithography. A cross-sectional diagram of the HEMT structure is shown in Figure 1.

III. Measurements

After fabrication, the 100 μm, 250 μm, and 400 μm total gate periphery, dual-gate "U"-layout devices were characterized on-wafer using coplanar waveguide probes contacting Ti/Au probe pads. DC and small signal measurements were taken, as well as large signal measurements on a 10 GHz CW harmonic load-pull system.

The small signal device parameter extraction measurements were taken using an HP 8510C, 50 GHz network analyzer, with DC bias supplied by an Agilent 4144B connected to the network analyzer bias tees. The combination of probes, cables, and connectors was calibrated from 500 MHz to 42 GHz using a co-planar impedance standard substrate [21].

After small signal characterization, power measurements were performed. A schematic of the large-signal measurement system is given in Figure 2. The 10 GHz signal was generated by an Agilent 83650 CW generator and then amplified by a 10 W amplifier. Bias was provided by an Agilent 4142B SMU through bias tees at the input of the input tuner and the output of the fundamental output tuner. Maury MT982 mechanical tuners were used as the input and fundamental output tuners, and one MT983 tuner was used for the second harmonic output. The fundamental and second harmonic outputs signals were separated by a diplexer with measured insertion loss of 0.21 dB. The fundamental output signal was attenuated by a 30 dB attenuator after the output tuner. The input and reflected signals were measured with an Agilent E4417A dual-channel power meter. A second Agilent E4417 was used to measure the fundamental and second harmonic output powers.

The first step of the matching process was setting the source impedance. The goal was to create a conjugate match to allow maximum power transfer from the source to the device. Therefore, the reflected power should be minimized. The matching

was done by first scanning the input tuner slide over the range of a wavelength to find the point where the reflected power was at a minimum. Then, the slide was scanned and again the point of minimum reflected power was taken. To verify a conjugate match, the connection was broken between the output of the input tuner and the input probes. Keeping all other connections, the one-port s-parameters were measured for the input into the device using the input probes, and the output of the input tuner looking backwards toward the source. These two sets of s_{11} measurements were mapped on a Smitch chart (Figure 3). A conjugate match at the output was measured in a similar fashion by breaking the connection at the output probe and measuring the s_{11} parameters looking into the output side of the device and the input side of output branch. (Figure 4). The effectiveness of the match is demonstrated by a power sweep (Figure 5).

The load impedance is usually set by the application, as the optimum tuning points for power, PAE, or gain may be different for the same device. In this case, the devices were tuned for maximum PAE. The output tuner was scanned in the same manner as the input tuner, except the point of peak efficiency was used instead of reflected power. Lastly, the load impedance of the second harmonic was set by scanning and optimizing the second harmonic tuner for maximum PAE.

IV. Results

A. Small Signal and DC Results

The pinch-off voltages of the SiN and AlSiN-passivated devices were approximately -2.5 and -1.5 V, respectively, while the as-grown pinch-off was -4 V. This indicates that the barrier layers were recessed by the gate window etch by differing amounts. Figure 6 shows the pinch-off voltages measured for both types of passivation as a function of gate length. The quiescent voltage was chosen as the point of maximum transconductance for all devices.

1) Parameter Extraction: Parameter values obtained using small signal model extraction as described by Shealy et al [11], as based on the Tasker and Hughes model [22]. The parasitic elements were extracted by biasing the devices at two operational extremes, approximating either a short or open circuit, which allows for the extraction of capacitive and inductive elements. The extraction was carried out over a range of biases, and the values in the bias-independent regions were used.

Devices with both types of passivation showed trends similar to previous work [11]. For both passivation schemes, small periphery devices exhibited lower parasitic capacitances, but higher series parasitic resistances. Gate resistance scaled inversely with gate length.

2) Performance of Dielectrics: Several significant differences in the small signal performance of the two dielectrics were observed. In particular, lower values for several key parasitics were observed for the AlSiN-passivated devices.

The access (source and drain) resistances were found to be comparable for both AlSiN- and SiN-passivated devices under standard extraction conditions. To observe the changes in access resistance with drain current, the gate voltage was swept from pinch-off into forward bias and the resistance values were extracted at each point. For both SiN and AlSiN, the drain resistance was bias-independent. However, the source resistance was found to increase non-linearly with drain current in the SiN-passivated devices. This effect is attributed to large longitudinal electric fields in the source-gate region [23]. As shown in Figure 7, the AlSiN-passivated devices did not exhibit this behavior, as both the source and drain resistances remained more or less bias-independent.

Another set of key parasitics that showed significant differences between the two passivation materials was the pad capacitance. Figure 8 shows the gate-drain pad capacitance for various periphery devices.

The AlSiN-passivated devices had consistently lower values across all peripheries. As will be discussed further, the gate-drain and gate-source pad capacitances affect or limit the f_T and f_{max} of the device.

3) Figures of merit: The maximum value of the extrinsic f_T recorded was 87 GHz, and the maximum value of the extrinsic f_{max} was 150 GHz. The f_T was optimized at a gate length of 75 nm, and f_{max} optimized at a gate length of 200 nm. The AlSiN coated devices consistently had roughly 10 % higher values of these device bandwidth metrics for the same gate dimensions. This is attributed to the reduction of key parasitics. Figures 9 and 10 show the trends of the extracted intrinsic f_T and f_{max} with gate dimensions for AlSiN-passivated devices. The intrinsic f_{max} maximized at the same gate length of 200 nm was 202 GHz for a 100 μm gate periphery. However, intrinsic f_T maximizes at gate lengths of 100 or 150 nm.

Furthermore, there is a clear trend of increasing f_{max} with decreasing periphery, which can be attributed to decreasing parasitic capacitances. For a gate width of 50 μm, we predict an intrinsic f_{max} of approximately 260 GHz (Figure 11).

In order to simulate the relative effects of individual parasitic elements, the value of the element was swept from zero to its extracted value and the intrinsic device simulation was run at each step. It was found that the gate-drain pad capacitance has a significant effect on both the f_T and f_{max}. The f_T is also strongly affected by the gate-source pad capacitance and source resistance, though as periphery increases, the gate-source capacitance has an increasingly dominant effect. For example, an f_T of 66 GHz was extracted for an AlSiN-passivated device with gate length of 0.15 μm and periphery of 100 μm. The f_T was simulated to increase to 83 GHz by zeroing the gate-drain pad capacitance alone, and increase to 91 GHz by zeroing the gate-source pad capacitance alone. Zeroing the source resistance alone increased the f_T to 74.5 GHz. For a 0.15 μm gate length, 250 μm periphery device, the f_T increased from 69 GHz to 102 GHz with the removal of the gate-drain pad capacitance alone, and 136 GHz with the removal of the gate-source pad capacitance alone. Zeroing the source resistance alone increased the f_T to 93 GHz. The f_{max} is affected by the output conductance and for smaller peripheries, the gate-drain pad capacitance dominates the decrease in f_{max}, but the effects of the gate resistance and output conductance increase with increasing gate periphery. A 0.25 μm gate length, 100 μm periphery device, the extracted f_{max} of 125 GHz increased to 262 GHz with the elimination of the gate-drain pad capacitance, but just 136 GHz with the elimination of the gate resistance, and saw no change with the elimination of the output conductance. However, a 250 μm periphery device saw an increase in f_{max} from 66 GHz to 87 GHz without the gate-drain pad capacitance, 80 GHz without the gate resistance, and 86.6 GHz without the output conductance.

B. Large-Signal Results

Large signal measurements were performed at 10 and 35 GHz on a number of 100 μm and 250 μm gate periphery devices. The input RF signal was swept to the highest power possible before the gate was driven into forward bias. In our measurements, the AlSiN-passivated devices consistently outperformed SiN-passivated devices of identical dimensions. Figure 12 shows a typical power sweep for identical devices with different passivations. Not only did the AlSiN devices produce more gain and higher efficiencies, the efficiencies dropped off less sharply with increasing drain bias. This is the principle difference of the

performance of devices using the two passivation technologies.

A series of power sweeps were performed with the drain bias increasing in steps of 1 V or 5 V, until the device failed. The results are summarized in Figure 13.

The drain bias range reflects the difference between the drain bias tolerance of the two passivations. The AlSiN-passivated devices were consistently able to perform at higher drain biases, as high as 55 V, while the SiN-passivated devices often broke down above 45 V.

Overall, the AlSiN-passivated devices consistenly out-performed the SiN-passivated devices. A maximum PAE of 82% was measured at 15 V on a 100 μm gate periphery, AlSiN-passivated device, with 24 dB of gain. The maximum output power measured was 17.5 W/mm at 55 V on the drain. For the SiN-passivated devices, the maximum PAE was 72.5 % at 15 V, with 20 dB of gain, and the maximum output power was 7.5 W/mm at 37 V on the drain.

The impact on efficiency has been of particular interest. In this setup, the termination of the second harmonic was achieved using a second tuner, which was adjusted to achieve maximum PAE. To study the effect of the second harmonic loading, a series of power sweeps were carried out at various tuner settings. First, it was confirmed that terminating the second harmonic in a short would maximize the output power and efficiency. When the tuner is "shorted", the probe is all the way down, or 0 mm "out". The distance "out" increases as the probe is pulled out to approximate an open. Figure 14 shows the second harmonic power as a function of the tuner slide position with varying probe positions. When the probe is brought close to the transmission line—approximating a short—the second harmonic power is observed to have its largest swing in value over the range of the slide. Furthermore, it is observed (Figure 16) that when the second harmonic power is at a maximum, the first harmonic power is at a minimum.

Next, the gate-source bias was swept from the quiescent voltage (the peak of transconductance) to close to pinch-off (Figure 15). For a 250 μm, SiN-passivated device, the PAE increased from 63 % at V_{gs} = -2.2 V to 70 % at V_{gs} = -3 V.

V. Conclusions

High efficiency HEMTs passivated using AlSiN have been demonstrated. An output power of 17.5 W/mm with a corresponding PAE of 61 % at 10 GHz has been shown at a drain bias of 55 V. These devices also maintained state-of-the art small signal performance, with close to 90 GHz extrinsic f_T, and 150 GHz extrinsic f_{max}. The AlSiN-passivated devices consistently out-performed their SiN counterparts in both small and large signal measurements.

VI. Acknowledgment

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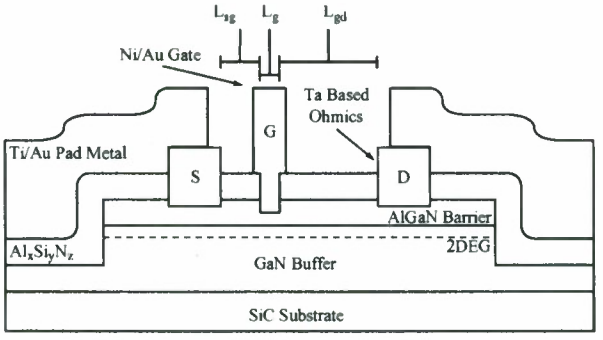

Fig. 1. Cross-sectional schematic of HEMT structure, showing design parameters.

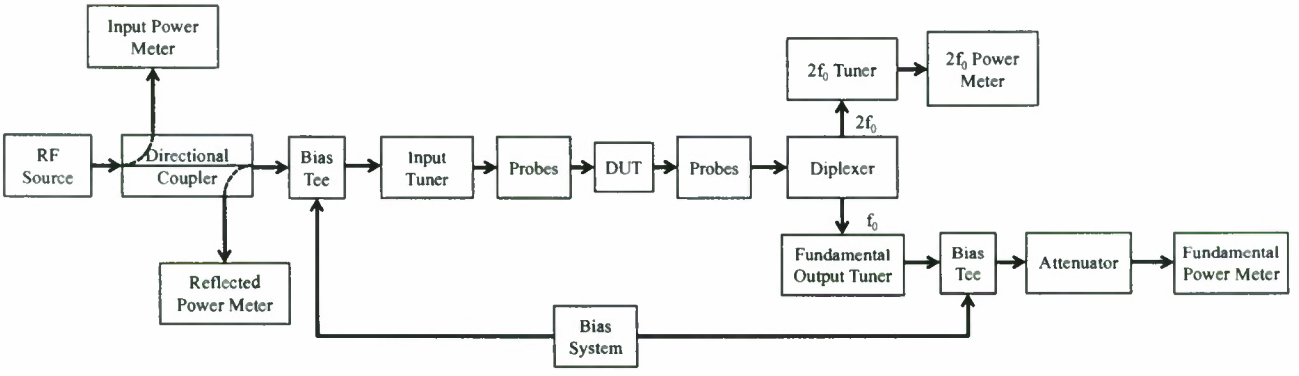

Fig. 2. Schematic of large signal power bench featuring a low loss diplexer to separate the 10 and 20 GHz components of the output signal.

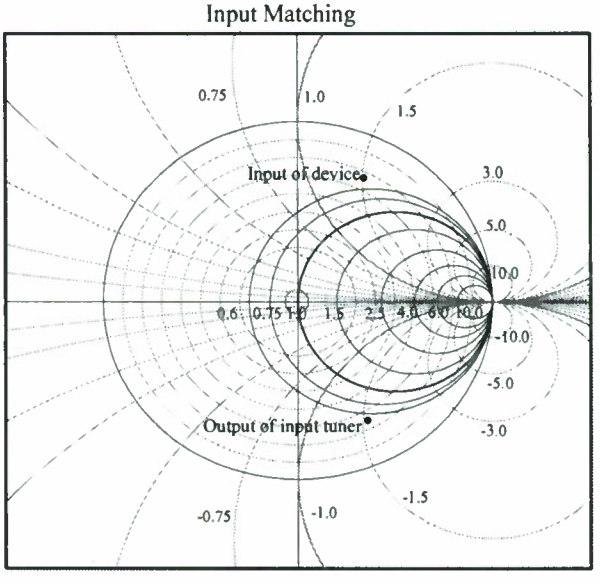

Fig. 3. S_{11} parameter looking into the device through input probes and looking back into the input tuner with a 100 μm gate periphery, 0.25 μm gate length device.

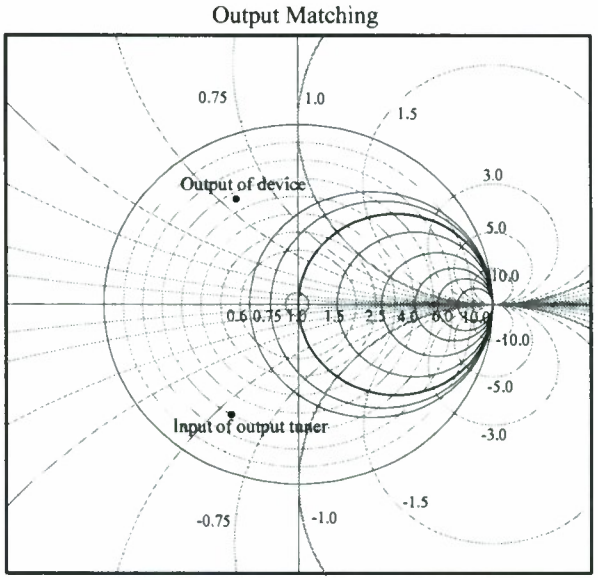

Fig. 4. S_{11} parameter looking into the device through output probes and looking into the output tuner with a 100 μm gate periphery, 0.25 μm gate length device.

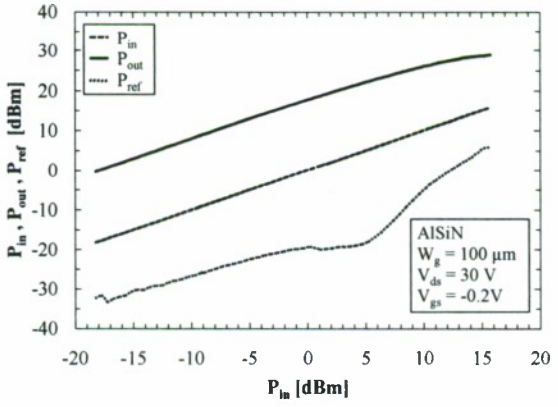

Fig. 5. Input, output, and reflected power with drive. Note the visible drop in reflected power at the drive at which the device was tuned.

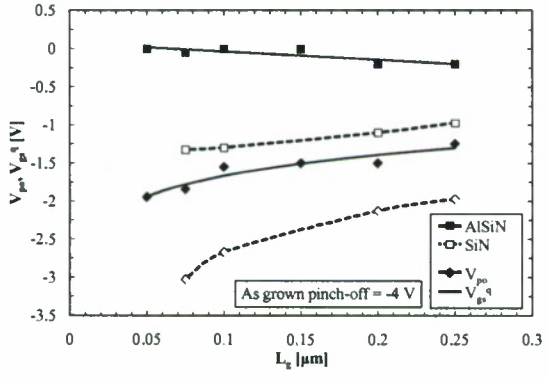

Fig. 6. Pinch-off and quiescent voltages of AlSiN and SiN passivated devices

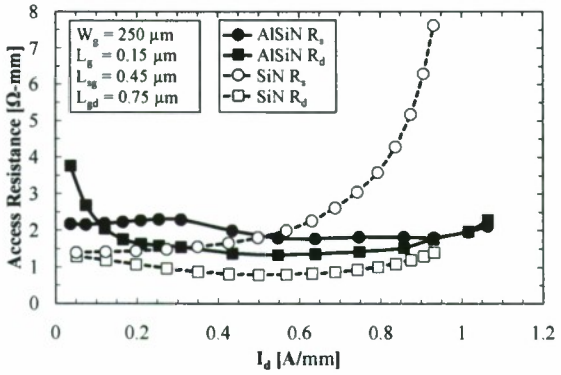

Fig. 7. Behavior of extracted access resistance as a function of drain current for devices of both passivation schemes. The SiN-passivated devices exhibit significant non-linearity at high drain currents.

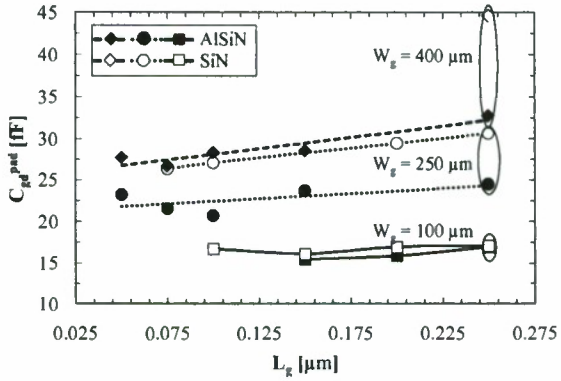

Fig. 8. Extracted gate-drain pad capacitance plotted against gate length and periphery.

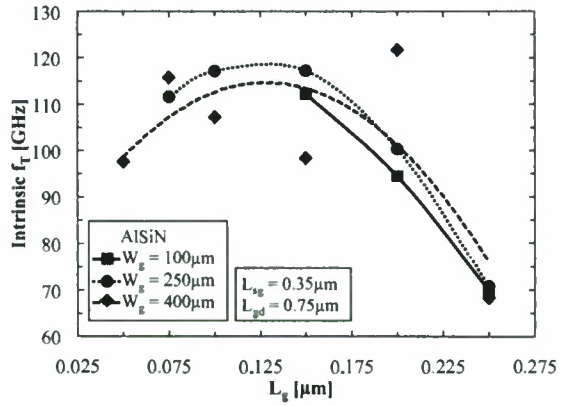

Fig. 9. Intrinsic f_T extracted against device gate length. As gate length decreases, the cut-off frequency increases to an optimum at a length of around 100 or 150 nm, beyond which the performance of the device begins to deteriorate.

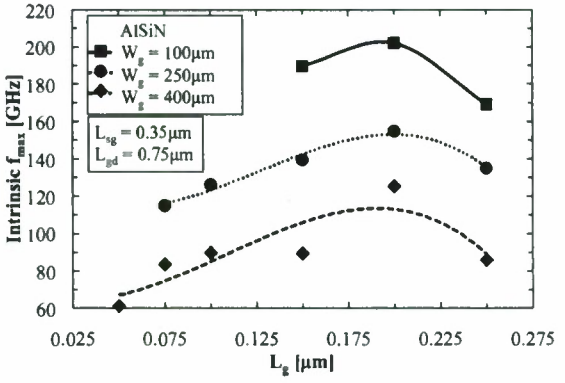

Fig. 10. Intrinsic f_{max} extracted against device gate length. As gate length decreases, the frequency increases to an optimum at a length of 200 nm.

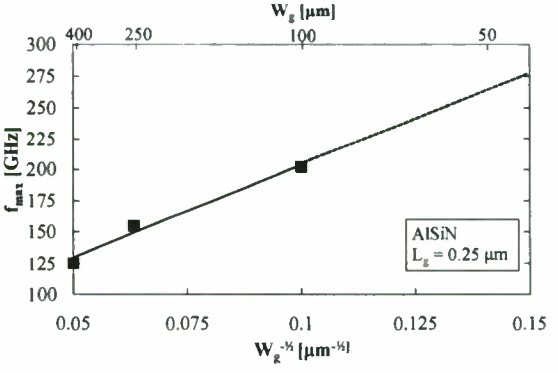

Fig. 11. Intrinsic f_{max} plotted versus inverse gate periphery.

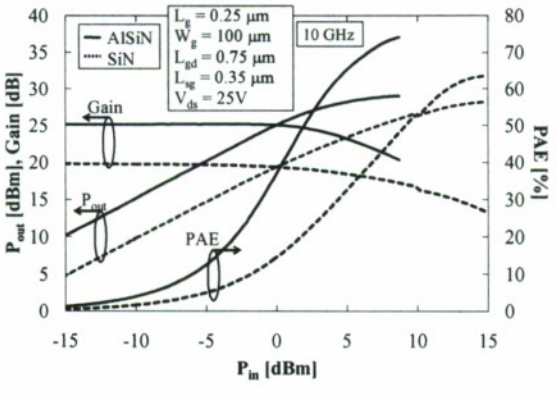

Fig. 12. Gain, output power, and power-added efficiency as a function of input power for 100 μm gate periphery, 0.25 μm gate length devices of both passivation schemes.

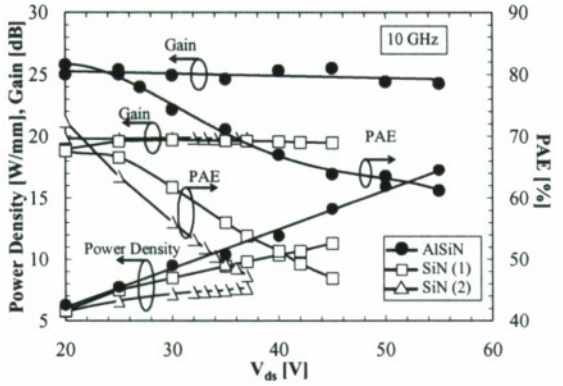

Fig. 13. Comparison of gain, PAE, and output powers for AlSiN- and SiN-passivated devices. SiN(1) refers to an earlier stand-alone sample fabricated by the same process as the SiN(2) and AlSiN samples, which were fabricated side-by-side.

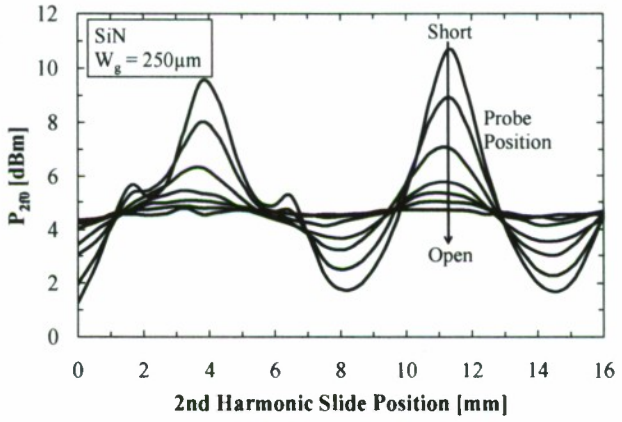

Fig. 14. Second harmonic output power as a function of the second harmonic tuner slide and probe. The probe position ranged from 2.222 mm to 0.3175 mm out. The device was biased at V_{ds}^{q} = 15 V, V_{gs}^{q} = -2.2 V, I_{d}^{q} = 62.27 mA

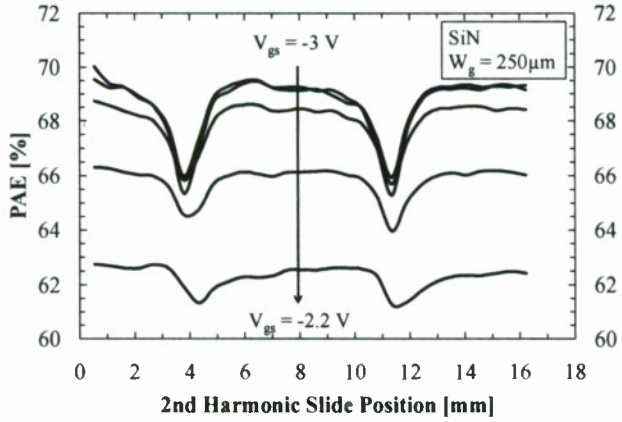

Fig. 15. Power-added efficiency as a function of gate bias and second harmonic tuner slide position. The second harmonic probe was fixed at 0.635 mm out, and the device was biased at V_{ds}^{q} = 15 V, V_{gs}^{q} = -2.2 V, I_{d}^{q} = 62.27 mA and driven at 11.54 dBm of input power.

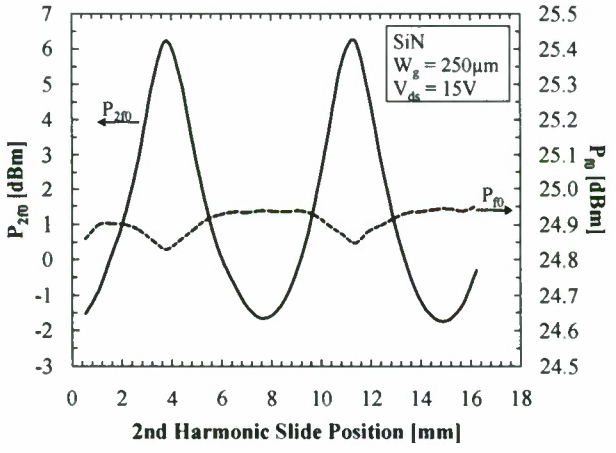

Fig. 16. Second harmonic output power and fundamental power as a function of the second harmonic tuner slide. The second harmonic probe was fixed at 0.9525 mm out, and the device was biased at $V_{d,s}^{q}$ = 15 V, $V_{g,s}^{q}$ = -2.2 V, I_{d}^{q} = 62.27 mA and driven at 11.54 dBm of input power.